AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-32 (Cancelled)

33. (New) A system comprising:

a processor;

a processor bus coupled to the processor;

a memory;

a memory control hub coupled to the processor bus and coupled to the memory;

a graphics accelerator coupled to the memory control hub;

a bus coupled to the memory control hub, the bus to transmit packets;

an input-output device; and

an input-output hub coupled to the bus and coupled to the input-output device, wherein the system is capable of passing messages between the memory control hub and the input-output hub through packets transmitted on the bus, the messages including information about signals received from one or more of the processor, the memory, and the input-output device.

34. (New) The system of claim 33, wherein the packets comprise a special cycle packet embodying virtual wire control information.

35. (New) The system of claim 33, wherein the packets comprise a special cycle packet encoding a command to assert a PHLD signal.

36. (New) The system of claim 33, wherein the packets comprise a special cycle packet encoding a command to act as if SERR# was received.

37. (New) The system of claim 33, wherein most of the control information for the bus is embedded in the packets.

38. (New) The system of claim 33, wherein the bus is capable of using a packet-based split-transaction protocol.

39. (New) The system of claim 33, wherein the bus is capable of using a source synchronous (SS) data transfer technique that is capable of being quad-clocked.

40. (New) A chipset comprising:

a memory control hub capable of being coupled with a processor and capable of being coupled with a memory;

a bus coupled to the memory control hub, the bus to transmit packets; and

an input-output hub coupled to the bus and capable of being coupled to an input-output device,

wherein the chipset is capable of passing messages between the memory control hub and the input-output hub through packets transmitted on the bus, the messages including information about signals received from one or more of the processor, the memory, and the input-output device.

41. (New) The chipset of claim 40, wherein the packets comprise a special cycle packet embodying virtual wire control information.

42. (New) The chipset of claim 40, wherein the packets comprise a special cycle packet encoding a command to assert a PHLD signal.

43. (New) The chipset of claim 40, wherein the packets comprise a special cycle packet encoding a command to act as if SERR# was received

44. (New) The chipset of claim 40, wherein the bus is capable of using a packet-based split-transaction protocol.

45. (New) The chipset of claim 40, wherein the bus is capable of using a source synchronous (SS) data transfer technique that is capable of being quad-clocked.

46. (New) A system comprising:

a first hub to receive a first signal;

a first hub interface coupled to the first hub, the first hub interface to receive a message that is passed from the first hub, the message corresponding to the first signal, the message including a packet including control information;

a second hub coupled to the first hub interface, the second hub to receive the message from the first hub interface.

47. (New) The system of claim 46, wherein the packet including the control information comprises a special cycle packet embodying virtual wire control information.

48. (New) The system of claim 47, wherein the virtual wire control information is in place of a wired sideband control.

49. (New) The system of claim 46, wherein the packet including control information includes a special cycle packet encoding a command to assert a PHLD signal.

50. (New) The system of claim 46, wherein the first hub interface is capable of using a source synchronous (SS) data transfer technique that is capable of being quad-clocked.

51. (New) The system of claim 46, further comprising:

a second hub interface coupled to the second hub, the second hub interface to receive the message from the second hub; and

a third hub coupled to the second hub interface to receive the message from the second hub interface, wherein the message includes control information to control the second hub and the third hub.

52. (New) An apparatus comprising:

a first component;

a bus coupled to the first component, the bus to transmit packets, the packets including special cycle packets embodying control information; and

a second component coupled to the bus, the second component to receive the packets from the first component via the bus.

53. (New) The apparatus of claim 52, wherein the special cycle packets embodying the control information comprise embody virtual wire control information.

54. (New) The apparatus of claim 52, wherein the special cycle packets embodying the control information comprise a special cycle packet encoding a command to assert a PHLD signal.

55. (New) The apparatus of claim 52, wherein the special cycle packets embodying the control information comprise a special cycle packet encoding a command to act as if SERR# was received.

56. (New) The apparatus of claim 52, wherein the bus is capable of using a packet-based split transaction protocol.

57. (New) The apparatus of claim 52, wherein the bus is capable of using a source synchronous (SS) data transfer technique that is capable of being multi-clocked.

58. (New) The apparatus of claim 52, wherein the first component comprises a memory control hub, and wherein the second component comprises an input-output hub.

59. (New) The apparatus of claim 58, further comprising:

a graphics accelerator and a memory coupled to the first component; and

a FLASH bios coupled to the second component.

60. (New) The apparatus of claim 52, wherein the control information includes control information to control an arbitration sequence.

61. (New) The apparatus of claim 52, wherein the control information includes control information to control transaction ordering.

62. (New) A method comprising:

receiving a signal at a first component;

passing a first message that encodes information relevant to the signal from the first component through a bus coupled to the first component, the first message including a special cycle packet including control information; and

receiving the first message from the bus at a second component.

63. (New) The method of claim 62, wherein the special cycle packet comprises information embodying virtual wire control information.

64. (New) The method of claim 62, further comprising:

checking the packet for a special cycle at the second component; and

if a special cycle is found, then processing the special cycle.

65. (New) The method of claim 62, wherein the packet comprises a request packet, and further comprising transmitting a completion packet after said receiving the first message in order to terminate a transaction.

66. (New) A method comprising:

receiving a first signal at a first hub coupled to a hub interface;

passing a message corresponding to the first signal from the first hub through the first hub interface, the message including a packet including control information; and

receiving the message from the hub interface at a second hub coupled to the hub interface.

67. (New) The method of claim 66, wherein the control information embodies virtual wire control information.

68. (New) The method of claim 66, further comprising:

checking the packet for a special cycle; and

if a special cycle is found, then processing the special cycle.

69. (New) The method of claim 66, further comprising:

determining if the message is intended for the second hub;

acting on the message if said determining indicates the message is intended for the second hub; and

passing the message through a second hub interface if the determining indicates the message is not intended for the second hub.